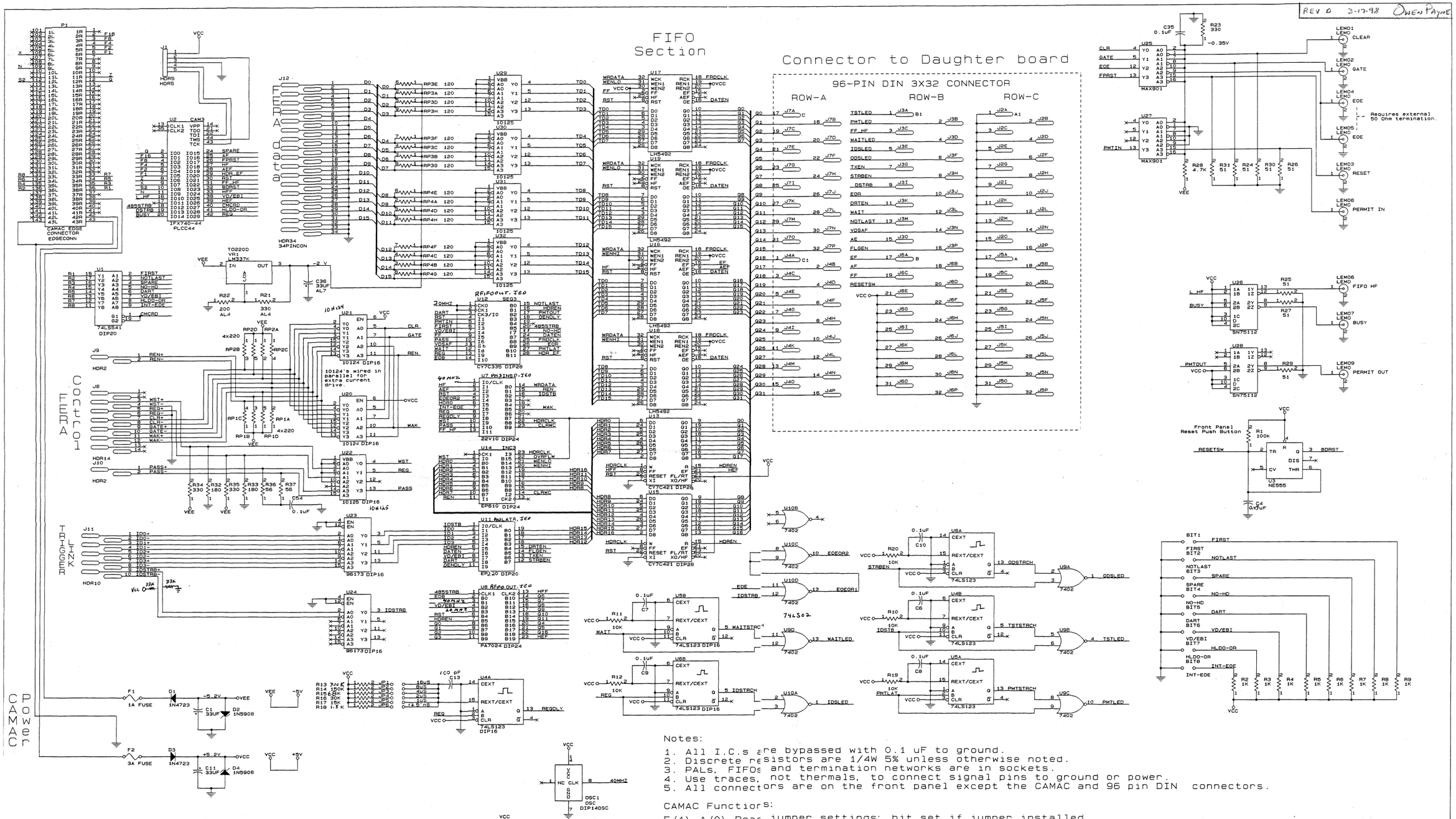
REV 0 3-17-98 OWEN PAYNE



Notes:

1. All I.C.s are bypassed with 0.1 uF to ground.
2. Discrete resistors are 1/4W 5% unless otherwise noted.
3. PALs, FIFOs and termination networks are in sockets.
4. Use traces, not thermals, to connect signal pins to ground or power.
5. All connectors are on the front panel except the CAMAC and 96 pin DIN connectors.

CAMAC Functions:

F(1) A(0) Read jumper settings; bit set if jumper installed.

BIT 8 INT-EOE, HLDO-OR, VD/EBI, DART, NO-HD, HF/AF, NOTLAST, BIT 1 FIRST

F(9) A(0) Reset module

Module does not assert LAM.

Module resets on C and Z.

Fermilab Physics Section

Requested by:
A. Kreymer / R. Tschirhart
Designed by: D. Graupman, S. Hansen
http://fnphyx-www.fnal.gov/elec/dyc.html

Title: DYC+ FERA bus to DART buffer interface

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