

CAMAC BUFFER MEMORYES-7078FUNCTIONAL DESCRIPTION

The NAL CAMAC Buffer Memory is a 64 word x 24 bit bipolar memory module mounted in a single width CAMAC package. Data words which are presented to the memory via a front panel or rear panel Data In connector can be strobed into the memory at 150 nsec intervals. Any number of units may be concatenated by a daisy-chain connection. A write counter (WC) points to the data word to be written next. The WC is automatically incremented on each successive data strobe. Inputs are TTL, with jumper selection for positive or negative logic.

The buffer memory is read out via the CAMAC dataway using normal CAMAC function reads (F0 or F2). Similar to the write counter, a read counter (RC) points to the next word to be read and is automatically incremented on each successive read.

THE WRITE OPERATION

A normal operation cycle of the buffer memory starts with a CAMAC F(26)·A(0) to enable the buffer memory. Next a CAMAC F(9)·A(0) and a F(9)·A(1) resets the Read Counter (RC) and the Write Counter (WC) respectively. The F(9)·A(1) command also resets the LAM. At this point the buffer contains no useful information. It should be noted that the WC may also be cleared by a TTL pulse via a front panel LEMO connector marked EXT or via a line in the 52 pin Data In connector (pin 52). A jumper option is available so that this pulse also clears the RC. The module to be made ready to accept data must have the WC enable LEMO input marked EN clamped to ground. A TTL pulse on pin 17 of the 52 pin Data In connector or the front panel push button C switch will reset both WC and RC and also enable the memory module. All TTL pulses utilized here are negative logic 50 nsec long pulses, i.e. normally > 3.5 volts going to ground for at least 50 nsec.

Data may now be presented via the Data In connector and strobed by bringing the WC strobe line (pin 51) low. This line must be kept low and the data remain static for at least 100 nsec. At the end of that time, new data may be presented, the WC strobe must go positive for at least 50 nsec and the process may then be repeated. With each strobe the WC is incremented by 1. The state of the WC is available as a LED display on the front panel. The data levels are TTL. A jumper selection allows for positive (1 for high) or negative logic (1 for low). Normally all options are supplied to the user wired for negative logic. The pin assignment for the Data In connectors are given in Table 1.