

RESEARCH DIVISION / RESEARCH FACILITIES DEPARTMENT

PROGRAMMABLE LAM MODULE RFD02

(DAN GRAUPMAN EXT. 3614)

This single-width CAMAC module is designed to act as a combination 8 bit Nim input-register, Lam generator, trigger-selector, master-inhibit and scaler. All front panel inputs and outputs are NIM. A 16 bit ECL input register with strobe is also available at the auxiliary rear connector.

The eight inputs can be enabled (via CAMAC or local switches) to cause a Lam to be generated on receipt of a Nim signal. Once an input which will produce a LAM is received, further inputs will be ignored (not generate further LAMs) until the module is reset (via CAMAC). The state of the inputs are latched at the time of the trigger and are available via a CAMAC read. An inhibit out is generated from the time of the receipt of the first enabled input until the LAM is reset and reenabled (via CAMAC). The auxiliary rear-connector contains a 17 pair input for ECL signals; the top 16 pairs are received in a latch which is strobed by the 17th pair. These inputs do not generate a LAM.

The following LAM, registers, counters and outputs are provided.

A register shows which inputs are "enabled". A nim signal of at least 20 nanoseconds on any enabled input will generate a LAM, if the LAM itself has been enabled. F(0) A(0) reads this register, F(16) A(0) writes it in "remote mode" or it is set by dip-switches in "local" mode. A front-panel switch selects the mode. LED's on the front-panel indicate which inputs are "enabled". A register shows the state of all the inputs 10ns after the first enabled trigger input. Read with F(1) A(0)..lower 8 bits, or F(1) A(2).

A LAM is generated when a signal is received at an enabled input. The LAM must be reset F(10) and reenabled F(26), or reset and enabled F(28), for further inputs to generate LAMs. There is a small delay (60 ns minimum, but which can be increased by installing a capacitor) between the receipt of the LAM re-enable and the actual re-enabling of the trigger inputs to prevent a new LAM being generated before the computer is really ready to receive one.

A 16 bit ECL input register and strobe is available at the auxiliary connector, the input register is a transparent D type latch which is latched after the occurrence of a pulse on the strobe input pins. This register can be read with F(0) A(1), and reset with F(9) A(1), or read and reset with F(2) A(1).

A counter counts the number of LAMS generated. It's read with F(1) A(0) R9-R16, reset with F(11) A(0), or read and reset with F(4) A(0). This allows a check that the computer sees the same number of Lams as the module generates. A counter counts the number of times any NIM signal is received (enabled or not). This counter is always live independent of whether a LAM is being processed or not, however the value of the counter is latched at the time a LAM is generated. After reset of the LAM the current value of the counter can be read. Read with F(1) A(1), reset with F(11) A(1), or read and reset with F(4) A(1). This allows a measure of live-time

A pulse \approx 60 ns wide is provided on the "TRIG OUT" when an input is received which will produce a LAM. This pulse is delayed by 20 ns from the triggering input.

Nim levels are provided on the INHIBIT OUTPUTS from the time that an enabled input is received until the LAM is reenabled.

An input "ENABLE IN" is provided to allow the module to be ENABLED by an externally applied NIM level. If an external enable is not being used "ENABLE IN" MUST be connected to "ENABLE OUT".

In a system that requires two modules, the ENABLE IN's should be cross-connected to the ENABLE OUT's. For the two modules to be reenabled simultaneously the output cable length should equal the delay time (delay from camac enable to actual enable) of the generating module.

Front panel description:

Local - Camac Switch : on front panel, enables trigger mask to be set via the dip switches on the board, or via CAMAC.

Inhibit out - lemo connector : nim output, equal to inhibit out, upper connector is active low, lower connector is active high.

Enable in - lemo connector : nim input. enables the trigger counter and lam generation. (active low).

Enable out - lemo connector : nim output from LAM is reenabled until receipt of valid trigger (active low).

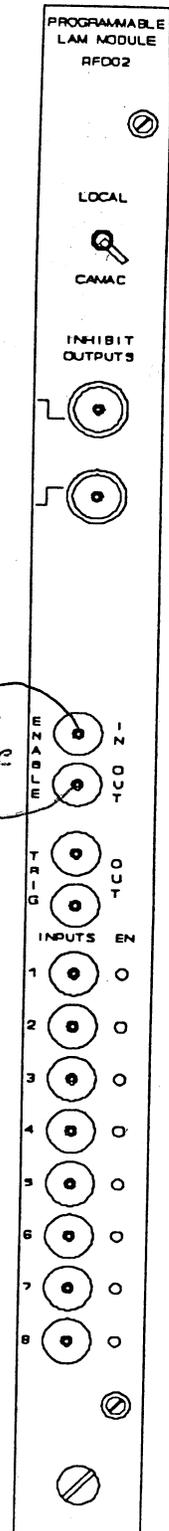
Nim out - lemo connector : nim output ≈ 60 ns signal generated on receipt of a valid trigger.

Nim inputs 1 thru 8 - 1 pin lemo connectors : nim trigger inputs, must be 20 ns wide minimum.

Camac Commands:

Camac op codes - return x and q immediately except F(16) A(0) when set to local control, and F(8) when a lam is not present.

- A F(0) A(0) : reads trigger enable-mask bit 1 thru 8.
- B F(0) A(1) : reads state of 16 bit ECL input register on rear.
- C F(1) A(0) : reads trigger latches bit 1 thru 8, reads trigger counter bit 9 thru 16.
- D F(1) A(1) : reads always-live counter bit 1 thru 16. If a lam is present the value corresponds to the value of the counter at the time of the valid trigger, including the valid trigger. If the lam has been reset, the value is the current value of the counter.
- E F(1) A(2) : reads trigger latches bit 1 thru 8 only, upper bits are zero.
- F F(2) A(1) : reads and reenables 16 bit ECL input register on rear.
- G F(4) A(0) : reads trigger latches bit 1 thru 8, reads and resets trigger counter bit 9 thru 16 (note the trigger latches retain the same value until the lam is reenabled, and a valid trigger occurs).
- H F(4) A(1) : reads and resets always-live counter.
 - F(8) : test lam.
 - F(9) A(1) : reenable 16 bit ECL input register on rear.
 - F(10) : clear lam.
 - F(11) A(0) : reset trigger counter.



F(11) A(1) : reset always-live counter.

F(16) A(0) : write trigger mask bit 1 thru 8, command not accepted when in local control.

F(24) : disable lam.

F(26) : enable lam, enables module after ≈ 60 nano sec.

F(28) : reset and enable lam, enables module after ≈ 60 nano sec.