

Technical Information

GENERAL DESCRIPTION

LRS Model 161/161L contains two high-speed pulse amplitude discriminators with operating characteristics specifically chosen for general purpose use in high energy physics applications.

Each of the channels delivers an output whenever a pulse at its input exceeds the fixed input threshold of -100 mV. A front-panel input impedance switch selects either a constant, matched 50Ω impedance or high impedance and two paralleled connectors to make the input signal available for further use in the system.

Input protection extends to ± 100 volts for pulses. An exclusive LRS Limiter Circuit provides direct coupling, temperature compensation, and input matching at all input amplitudes.

The wide-band, direct-coupled input circuit design makes the threshold virtually independent of input shape and duration, thus permitting its use both with nanosecond pulses from fast photomultipliers and with slower pulses from other sources.

Each channel of the 161 has a separate high-speed inhibit input which may be used to veto any discriminator output. The inhibit circuit is of the leading edge type and the duration of the inhibit need only overlap the leading edge of the discriminator input to prevent an output.

Both channels of the 161 may be gated off by means of the NIM bin gate. The bin gate enters the module via the rear multipin connector and a rear panel On-Off switch. Quiescently at ± 5 volts, the bin gate line must be clamped to ground to inhibit the discriminators. The bin gate is direct-coupled, and has rise and fall times of approximately 50 ns.

Once triggered by a signal whose leading edge crosses the preset threshold value, the 161 generates three NIM fast logic outputs. The positive output, or complement, is quiescently at a logical one state (-32 mA or 1600 mV into 50Ω) and switches to 0 mA (or 0 volts) for the duration of the output. Each of the two negative outputs consists of two paralleled BNC connectors driven from a common -32 mA current source. These outputs are quiescently at zero and switch to -800 mV (if both outputs drive 50Ω) during an output. The incorporation of two paralleled output connectors permits the negative signal to be clipped, back-terminated, or fanned-out to two 50Ω loads.

Technical Information

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The duration of the output is determined by the output mode selected by a two-position front-panel control. In the Normal setting, the duration is set by a front-panel potentiometer and a three-position range switch. It may be set continuously from 3 to 150 nanoseconds and is independent of input duration, amplitude, and rate. In the DC Pass setting, the output duration is equal to the preset duration or the duration of the input pulse, whichever is longer. Operation in this mode also causes the output to remain in its "1" state for the duration of any input pulse burst of frequency too great for the unit to follow. This provides exceptional efficiency in "anti" applications by permitting the unit to achieve 100% duty ratio even in response to inputs that exceed its maximum rate capability.

The Model 161 is a deadtimeless or updating discriminator, and will respond to input signals even when an output is already present. The minimum pulse pair separation is under 6 ns for an equivalent CW rate of greater than 160 MHz. If the second pulse is received during the time the output from the first pulse is being produced, the unit will extend the output duration to reflect the occurrence of the second signal. The net output pulse, being the logical sum of two standard output pulses, is of standard amplitude, and retains the time information contained in the input signals.

The Model 161 offers non-multiple-pulsing operation to assure unambiguous response to input pulses regardless of their amplitude or duration. The 161 will not produce multiple output pulses even with input pulses that substantially exceed the input pulse in duration.

Technical Information

SPECIFICATIONS

- Number of Channels:** Two, both identical.
- Input Threshold:** -100 mV, fixed. The standard pulse used to calibrate threshold is 5 ns FWHM with rise and fall times of 2.0 ns.
- Input Impedance:** $50 \Omega \pm 5\%$ or one kilohm, switch selected; value of impedance is constant up to the limit of input protection.
- Input Protection:** ± 100 volt protection for pulses. D.C. overload characteristics are determined by the 500 mW dissipation limit of the 50Ω input terminating resistor.
- Input Coupling:** Direct-coupling assures a threshold value which is constant, independent of input risetime, duration, and rate.
- Input Reflections:** Dependent upon input risetime; less than 10% for input signal of 2 ns risetime or greater.
Note: The low minimum threshold of the 161 may be retriggered on reflections if pulse source is not back-terminated and maximum input amplitudes exceed 10 X threshold. Care should be taken to terminate source in 50Ω if such circumstances exist.
- Threshold Stability:** Input threshold temperature coefficient is $0.2\%/^{\circ}\text{C}$ over 20°C to 60°C operating range.
- Bin Gate:** Discriminators may be inhibited by application of NIM Bin Gate. Bin Gate enters module via pin #36 of rear multipin connector. Switch located on back panel disconnects 161 from Bin Gate line. Clamping Bin Gate to ground from ± 5 volts inhibits. Clamping circuit must sink 1.4 mA per module. Bin Gate circuit is direct-coupled. Rise and fall times are 50 ns.

-3-

Technical Information

SPECIFICATIONS

- Inhibit Input:** Leading edge; -350 mV threshold; direct coupled; 50 Ω impedance; rise and fall times 2 ns.
- Negative Outputs:** Two sets of paralleled connectors driven by common high impedance current sources. Quiescently, 0 mA, current sources switch to -32 mA during output. Unused outputs should always be loaded by 50 Ω by back-terminating, splitting, or clipping to assure proper adherence to specifications.
- Positive Output:** One, complementary, two paralleled connectors, quiescently -32 mA (1600 mV into 50 Ω load), switching to zero volts during an output; back-terminated; if unused, should be terminated in 50 Ω to assure proper adherence to specifications.
- Output Duration:** 3 ns FWHM to 150 ns, continuously adjustable by means of front-panel 10-turn width control and 3-position range switch (3-15, 12-50, 35-150). In DC pass, duration equal to input duration or preset duration, whichever is longer.
- Output Jitter:** <30 ps on shortest widths.
- Output Rise and Fall Times:** 1.5 ns typical, 10% to 90%; fall time slightly longer on wider widths.
- Output Duration Stability:** Less than 0.2%/ $^{\circ}$ C from 20 $^{\circ}$ C to 60 $^{\circ}$ C.
- Time Resolution:** When two Model 161 channels drive two inputs of a logic unit, counting rate is down by a factor of 100 in 60 ps at either end of coincidence curve.
- Double Pulse Resolution:** Minimum separation to resolve two pulses is typically under 6 ns. Double pulse resolution is a function of output width as defined by the approximate relationship $T_0 / 2 + 5$ ns where T_0 is output pulse duration.