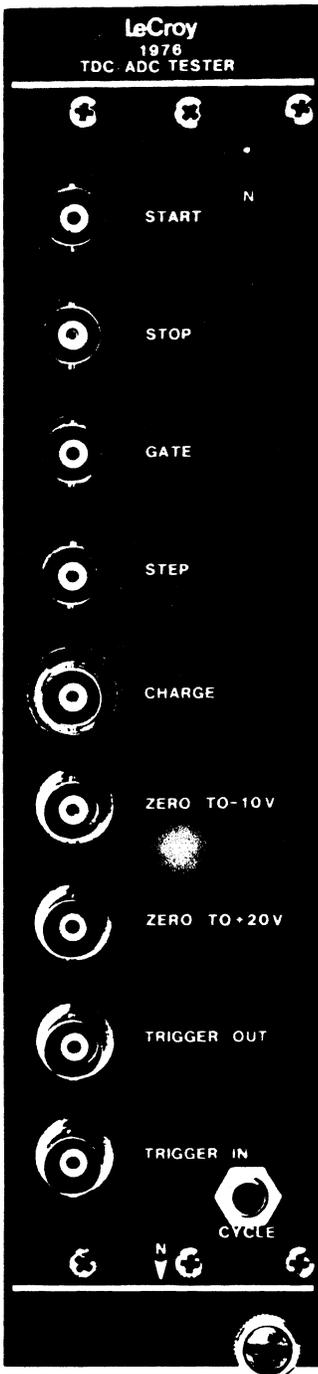


LeCroy

CAMAC Model 1976 ADC/TDC Tester



The LeCroy Model 1976 is a programmable pulse generator packaged in a #3 CAMAC module. It has been designed as a test instrument useful for servicing ADC's and TDC's of the type manufactured by LeCroy. With it, linearity and resolution measurements can be made on TDC's and current-integrating ADC's. In conjunction with the Model 1516 Shaper-Amplifier it can also be used to test peak-sensing ADC's.

The Model 1976 has front-panel BNC outputs to accommodate each of the test modes. For ADC calibration, separate outputs are provided which supply a CHARGE pulse, a voltage STEP, a positive DC level, and a negative DC level. Peak signals are derived from the voltage step output using the LeCroy Model 1516 Peak-Shaping Amplifier. A NIM standard GATE output allows the ADC under test to be strobed or gated. NIM standard START and STOP outputs are also supplied for TDC calibration.

The pulse generator circuits of the Model 1976 are driven by a pair of digital-to-analog converters (DAC's). The output pulse amplitude or time interval programming precision is 16-bits, whereas an 8-bit DAC is used to determine the gate width.

The operating mode of the Model 1976 is defined by a 13-bit control word. This allows the charge, peak (when used with Model 1516), or time-interval mode to be selected. It also specifies the full-scale for each mode. CHARGE pulse shape and the width of the START and STOP pulses are also defined in this way.

The Model 1976 contains three registers called GATE TIME, AMPLITUDE, and CONTROL. The information written into them uniquely defines a test cycle which is executed 5 msec after the AMPLITUDE word is written into the Model 1976. A cycle may also be initiated by application of a TTL pulse at the front-panel trigger input. A front-panel cycle button can be used to initiate repetitive cycling at 100 Hz rate. Each cycle is preceded by a trigger output to facilitate interrogation of the signal outputs.

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SPECIFICATIONS

CAMAC Model 1976

ADC/TDC TESTER

OUTPUT CHARACTERISTICS

CHARGE

Front-panel BNC connector shield is AC-coupled to chassis ground. Output impedance is 50 ohms. Supplies a signal similar to a photomultiplier pulse with falltime selectable under CAMAC control. See options below. Charge output should be disabled when not in use in order to avoid crosstalk with other outputs. The risetime is <6 nsec, but smaller outputs are significantly faster.

Programming Options:

	Fall Time (90% to 10%)	
Full Scale	Fast Tail	Slow Tail
300 pC	15 nsec	350 nsec
600 pC	35 nsec	600 nsec
1200 pC	65 nsec	1200 nsec

See Control Word Breakdown Table under CAMAC OPERATIONS for Mode Selection.

Full-Scale Accuracy:

±2%.

Linearity:

<0.05% of full scale.

Amplitude Temp. Coef.:

<0.003%/°C (25°C to 50°C).

Noise:

<0.1 pC (rms).

Load Impedance:

50 Ω ± 1%.

STEP

Front-panel BNC connector, DC-coupled, supplies a negative-going transition of maximum amplitude of 1.0 V with a 10-90% risetime of 10 nsec from a quiescent level of +0.7 V. Load impedance should be 50 Ω. Step output should be disabled when not in use to avoid crosstalk with other outputs.

GATE

Front-panel BNC connector. NIM current source outputs parallel-terminated with 50 Ω. Drives a 50 Ω load to -800 mV with risetimes and falltimes of <2 nsec. (10% to 90%). Leading edge precedes the CHARGE pulse by 15 nsec and the STEP output by 35 nsec.

Programming Options:

Pulse width equal to the START-STOP interval +10 nsec. See below. Normally programmed via the 8-bit DAC. See Control Word Breakdown Table under CAMAC OPERATION for Mode Selection.

START/STOP

Front-panel BNC connector NIM current-source outputs parallel-terminated with 50 Ω. Risetimes and falltimes <2 nsec. Delivers -800 mV into a 50 Ω load.

Programming Options: (See CAMAC OPERATIONS section for Mode Selection.)

Pulse Width	Full Scale Time	DAC Selection
20 nsec	150 nsec	8-bit ¹
100 nsec	300 nsec	16-bit ²
	600 nsec	
	1200 nsec	
	2400 nsec	
	4800 nsec	
	9600 nsec	

¹8-bit normally for ADC gate width studies.

²16-bit normally for TDC studies.

Full-Scale Accuracy: $\pm 2\%$.
Linearity: 0.05% of full scale.
Temperature Coefficient: $<0.005\%/^{\circ}\text{C}$ (25°C to 50°C)
Time Jitter: <20 psec (rms) for 150 nsec scale. Proportionally greater for longer time ranges.

NEGATIVE DC LEVEL Front-panel BNC connector. DC level set by the 16-bit DAC. Amplitude 0 to -10 V. Intended to drive $\geq 500 \Omega$.

Full-Scale Accuracy: $\pm 0.5\%$.
Linearity: $<0.005\%$ of full scale.
Temperature Coefficient: $<0.001\%/^{\circ}\text{C}$ (25°C to 50°C).

POSITIVE DC LEVEL Front-panel BNC connector. DC level set by the 16-bit DAC. Amplitude 0 to $+20$ V. Intended to drive $\geq 500 \Omega$.

Full-Scale Accuracy: $\pm 0.5\%$.
Linearity: $<0.005\%$ of full scale.
Temperature Coefficient: $<0.001\%/^{\circ}\text{C}$ (25°C to 50°C).

TRIGGER OUT Front-panel BNC connector supplies a 35 nsec wide 300 mV pulse into 50Ω . AC-coupled TTL negative-going edge (510 ohm in series with $0.01 \mu\text{F}$.) Precedes the leading edge of the gate by approximately 50 nsec. (Proportional to the full-scale time range selected.)

CONTROLS

CYCLE BUTTON: A front-panel pushbutton initiates cyclic operation. The operation is defined by CONTROL, GATE, and AMPLITUDE words. Repetition rate 100 Hz. Cycling is terminated when the module is addressed via the data-way.

TRIGGER INPUT: Front-panel BNC connector. TTL level (2.5 mA sink). A positive-going edge initiates one cycle as defined by the CONTROL, GATE, and AMPLITUDE words. A TTL low level will inhibit execution of a pulser cycle normally initiated by CAMAC F(16)•A(0) command. Maximum rate 200 Hz.

DAC 8 (Gate Register): An 8-bit DAC programmable via CAMAC command. May be selected to drive the TIME circuitry using CONTROL word bit W8. Normally used in this way to select gate width.

DAC 16 (Amplitude Register): A 16-bit DAC programmable via CAMAC command. Drives the AMPLITUDE circuitry. May be selected to drive the TIME circuitry (W8=0). Both POSITIVE LEVEL and NEGATIVE LEVEL outputs track this DAC.