

TECHNICAL DATA



SPECIFICATIONS
LeCROY MODEL 2285 24-CHANNEL ADC

INPUT SENSING:	Charge (Current-integrating).
ADC RESOLUTION:	12-Bits.*
FULL SCALE:	-400 pC.*
GAIN:	-10 counts/pC $\pm 10\%$ *
INPUT IMPEDANCE:	$50\Omega \pm 5\%$ 0 to -50 mA.
INPUT PROTECTION:	$\pm 50V$ for 1 μ sec transients.
INPUT LIMITATIONS:	Maximum voltage for linear response, -1.5 V. For 3 V max, input linearity is degraded to typically $\pm 1\%$ of reading ± 0.25 pC.
INTEGRAL LINEARITY:	Typically $\pm(0.1\%$ of reading ± 0.25 pC); Worst case $\pm(0.25\%$ of reading ± 0.5 pC) for signals of slew rate ≤ 2 mA/nsec. For signals of slew rate 4 mA/nsec, linearity is degraded to typically $\pm 1\%$ of reading ± 0.5 pC.
DIFFERENTIAL LINEARITY:	Typically 10% variations between odd and even readings. (i.e., variations in "bin widths" of $\approx 10\%$).
RESIDUAL PEDESTAL:	Typically 50 pC (subtracted from data by processor) for a gate width of 200 nsec and a high source impedance.
PEDESTAL-GATE WIDTH COEF.:	$\leq \pm 250$ fC/nsec for gate widths > 100 nsec.
TEMPERATURE COEFFICIENT:	Typically $(\pm 0.1\%$ of reading $\pm .001\Delta t$ counts)/ $^{\circ}C$ where Δt = gate width in nsec.
LONG-TERM STABILITY:	$\pm 0.25\%$ of reading $\pm .5$ pC/week at constant temperature and voltage.
CONVERSION TIME:	200 μ sec nominal + 18 μ sec per ADC module.
ANALOG INPUT CONNECTOR:	4 per module. LeCroy model CK6B or AMP model 226651-6 bulkhead mounting 6 pair connector. Mates with LeCroy CK6C (CK6B plus multicoax cable terminated at both ends with CK6C is available as part number DK6-length. Employs AMP model number 226298-6 six signal cable).
ADC ISOLATION:	> 60 dB. Including the effects of the CK6B input connector
GATE INPUT:	One per module, rear-panel input driven from nonregenerative driver (via ASB) in 2280 system processor module.
GATE WIDTH:	100 nsec to 500 nsec. Wider gates to 1 μ sec at the expense of increased pedestal.
GATE TIMING:	The gate input to the 2280 system processor opens the ADC gates 30 nsec after gate is applied. Gate inputs must precede the analog input by > 15 nsec.

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FAST CLEAR:

DIGITAL CLEAR:

TEST FEATURE:

ANALOG OUTPUTS:

**READOUT AND CONTROL:
PACKAGING:**

POWER REQUIREMENT:

May be executed any time. Settles from full scale to within 1 count within $\leq 1.5 \mu\text{sec}$.
 A digital clear is automatically generated by a fast clear $> 6 \mu\text{sec}$ after the gate. Requires 3 μsec .
 Exercised by 2280 system processor in response to a CAMAC F(25). All channels have a test pulse applied. The amplitude of the pulse is proportional to a DC level applied to the Test Input (0 to +10 V). Channel-to-channel matching of the test pulse is $\pm 10\%$. Requires a gate width of $> 300 \text{ nsec}$.
 Current outputs of proportional to input (-1 mA/-125 mV) available at each hybrid for summing by user. Risettime $> 10 \text{ nsec}$, 10-90%. Three output buffers on rear-panel allow option for additional current summing. Gate feed-through is $< 40 \mu\text{A}$ per channel.
 Requires one Model 2280/85 per CAMAC crate.
 No. 1 RF-shielded CAMAC module conforming to ESONE Report EUR 4100 and IEEE Standard 583.
 +6 V @ 700 mA +24V @ 60 mA
 -6 V @ 325 mA -24V @ 0

***Special Options:**

15 bit operation and variable gain. Specially modified system processor allows 15 bit conversion in 1.7 msec. Side panel accessed jumpers allow external voltage-programming of ADC gain over the range 7 to > 20 counts/pC. Voltage range: +20 to +6V. CAUTION: Sensitivity should be selected to give a full scale of 1000 pC or less.

Specifications subject to change without notice.

**PRELIMINARY
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