

Technical Information

GENERAL DESCRIPTION

The Model 2550B Quad 100 MHz Scaler is a single-width CAMAC module containing four 24 (or 16) bit scalars. Front-panel LEMO (or BNC) connectors are used for the signal, fast inhibit, and clear inputs. Also provided are a common "Clear" switch which resets all channels in parallel and a CAMAC "Inhibit Disable" switch which allows the CAMAC "I" command to be disregarded by all channels. IC sockets are used throughout. Requires approximately 8 W of ± 6 volt power.

Two bridged high impedance ($> 1 \text{ K}\Omega$) inputs on the front panel provide a common fast inhibit. An impedance of 50Ω may be obtained by simply terminating one of the inhibit inputs into 50Ω or by installing a 50 ohm resistor in the R_I location on the p.c. board. The inhibit must overlap the entire input pulse.

A front-panel 50Ω clear input, requiring a NIM-level, $> 100 \text{ ns}$ pulse, is provided to enable simultaneous clearing of all scaler channels from an external signal. In addition, front-panel light-emitting diodes (LED's) indicate the state of both the "N" line and of the scaler input gates.

The Model 2550B responds to the CAMAC function codes F0, F2, F9, and F25. F0 or F2 ("Read") and F2 or F9 ("Clear") commands may be used to control individual scaler channels. F25 is a test mode used to simultaneously test all counting registers in one module. Each counting register increments by 1 at the end of S_2 . The CAMAC "Q" response is generated in recognition of a F0, F2, F9, or F25 function for a valid "N" and "A".

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Specifications

Signal Input (each channel)	Threshold: Adjustable from -250 mV to -550 mV. Impedance: 50 Ω direct-coupled. Reflection: >10% typical at 1 ns risetime. Protection: \pm 50 volt transients. Minimum Pulse Width: 3.5 ns. Multiple Pulse Resolution: 10 ns. Counting Rate: DC to 100 MHz.
Signal Inhibit	Two bridged connectors, -500 mV threshold, width equal to Input (5 ns minimum), impedance > 1 K Ω . Inhibit pulses will not be counted by scaler.
Overflow Output	TTL open collector outputs available for connection to patch pins supply nominal usec wide clamp-to-ground pulse when scaler overflows. Soldered wire jumper on p.c. board provides option of causing last bit of each channel to remain set until channel is cleared.
Manual Clear	Front-panel switch allows clearing of scaler channels.
Front-Panel Clear	Same as Inhibit input except single connector; minimum width 100 ns.
Scaler Characteristics	First bits use discrete components and ECL integrated circuits. Remaining bits are TTL integrated circuits. Total capacity is 24 binary bits (16,777,216).
Manual Inhibit Disable	Front-panel switch provides the ability to disconnect the CAMAC "I" without disabling F25 or front panel Inhibit.
CAMAC Commands	Z or C: All Scaler channels are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. (Requires S ₂). I: All Scaler inputs are simultaneously inhibited for duration of CAMAC "Inhibit" command. This inhibit can be manually disabled by a front-panel switch. Q: A Q=1 response is generated in recognition of a F0, F2, F9, or F25 function for a valid "N" and "A", but there will be no response (Q=0) under any other condition.