

CAMAC Model 4300 B

16 Channel, Fast Encoding and Readout ADC (FERA)



- **High density:** 16 channels in a single width standard CAMAC module.
- **Fast conversion:** 11 bits in 8.5 μsec or 10 bits in 4.8 μsec .
- **High sensitivity:** 11 bits, 480 pC full scale; 10 bits, 256 pC full scale.
- **Floating common signal ground:** to eliminate sensitivity to common mode noise (hum) and DC offset.
- **50 Ω input impedance:** compatible 50 Ω multicoaxial flat cables.
- **Pedestal compensation:** minimizes the gate width effect on the pedestal.
- **Internal pedestal memory:** programmable pedestal subtraction during readout.
- **Programmable zero suppression or zero and overflow suppression:** compresses data and accelerates readout.
- **Programmable high speed readout:** 100 nsec/word via front panel ECL port.
- **Sequential or random access CAMAC readout.**
- **Common test feature.**
- **System compatibility:** designed for operation with fast buffer memories, bit slice processors, look up memories, data stacks and other ECL trigger processing units.

The LeCroy Model 4300 B Fast Encoding and Readout ADC (FERA) is designed to cover applications where charge measurements and readout must be performed rapidly and with high resolution. The FERA may be used as a single standard CAMAC module, or as part of a large system.

The FERA is a high speed charge integrating analog-to-digital converter. Each module contains 16 independent ADCs that are enabled by a common gate of 50 nsec to 500 nsec duration. Larger gate widths are possible after pedestal adjustment. The inputs offer a common mode rejection of ± 200 mV.

After conversion, the digitized data may be automatically corrected for pedestal with values contained in the internal programmable pedestal memory. Digitized data is available first on the front panel ECL port and, subsequently on the CAMAC dataway. The ECL port readout is optional. All zero or zero and overflow data words may be suppressed separately for the ECL port or CAMAC readout to provide data compression. The compression procedure requires 2.5 μsec (both after the conversion and ECL port readout).

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The front panel bus system includes the protocol necessary to permit high speed sequential readout to ECLine compatible modules including the LeCroy Models 2375 Data Stack Module, 2372 Memory Lookup Unit, and 4302 Triple Port Fast Memory. The Model 4302 is the memory extension of the LeCroy 4800 series of Fast Bit Slice CAMAC Processors which permits the distribution of programmable intelligence within the CAMAC system.

The analog inputs are also compatible with the outputs of Model 4303, Time to FERA Converter. These two modules together allow the implementation of a high resolution Fast Encoding and Readout TDC (FERET).

The readout modes, pedestals and remote testing of the Model 4300 B FERA are controlled via CAMAC. The gate, fast clear, test signals and ECL port timing for up to a crate of FERAs, may be controlled from a Model 4301 FERA Driver.

SPECIFICATIONS

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ANALOG INPUTS (16)

Connector:	17 × 2-pin front panel connector (BERG 75789-101-34). The upper 16 pins of the left row are negative signal inputs. The upper 16 pins of the right row are connected to the common virtual ground (AC coupled to ground). The lowest 2 pins are connected to ground.
Input Sensing:	Charge (current integrating).
Full Scale:	256 pC (10 bits), 480 pC (11 bits).
ADC Resolution:	Two factory options: 10 or 11 bits; the 10/11-bit selection is made via 4 internal jumpers and adjustment by an internal potentiometer.
Conversion Time:	Typically 10 bits in 4.8 μsec, 11 bits in 8.5 μsec.
Range:	10 bits typically 256 pC minus ADC pedestal. 11 bits typically 480 pC minus ADC pedestal.
Sensitivity:	10 or 11 bits 0.25 pC/count ± 3%.
Input Impedance:	50 Ω ± 3%, within the range of 0 to -60 mA DC. Above this limit, diode protection clamping will affect input impedance.
Input Protection:	± 25 V for 1 μsec transients (clamping diodes to ground and -3 V).
Input Limitations:	Maximum current for linear response -30 mA. With 50 Ω input impedance, the linearity is degraded to typically ± (1% of reading + 0.25 pC) for -60 mA.
Common Mode Properties:	Common mode rejection ratio > 50 dB for ± 200 mV (DC to 1 kHz).
ADC Isolation:	> 50 dB.
Integral Linearity:	Typically ± 0.5 pC. Worst case ± (0.25% of reading + 0.5 pC) for signals of slew rate < 2 mA/nsec. For signals of slew rate 4 mA/nsec, linearity is degraded to typically ± (1% of reading + 0.25 pC).
Differential Linearity:	Typically ± 10%, worst case ± 20%.
Residual Pedestal:	Minimum 1 pC and maximum 13 pC for a gate width from 50 to 500 nsec and all inputs open. Adjustable with an internal potentiometer for gate width > 500 nsec. Subtracted from data by CAMAC command.