

## DESCRIPTION

The CR116 is a 16 channel very high speed coincidence latch in a single width CAMAC module. Each channel is capable of responding to a coincidence overlap of 1  $\mu$ sec. between the leading edge of the data signal and a common strobe input. Detected coincidences set high speed latches which may then be read out on the Dataway on command. The strobe also sets the LAM status flip flop.

All inputs are standard 50 ohm NIM logic levels implemented with high speed ECL integrated circuits. To eliminate rate effects, the unit is entirely DC coupled and all inputs provide a high degree of protection against overload and low reflections.

A front panel clear input is provided to reset the data registers and LAM Status from an external source.

## APPLICATION

This module is primarily used in high energy nuclear physics for pattern recording of hodoscope and spark chamber arrays.

## FEATURES

- \* 16 channels in single width module,
- \* Minimum overlap time: 1  $\mu$ sec.,
- \* Pulse - pair resolution  $> 10 \mu$ sec.,
- \* Standard NIM logic levels, D C coupled,
- \* LED displays for N, L, and L Enable.

## Technical Specifications

### MECHANICAL

Single width unit, fully shielded,  
Weight 1 lb., 8 oz.,  
Operating temperature, 0-50° C at less than 80%  
humidity,

### ELECTRICAL

Input Current Thresholds--NIM levels,  
Input Impedance--50 Ohms,  
Power Requirements--±6 Volts,  
6.7 Watts,

### SIGNAL

Double pulse resolution, 10 nano seconds,  
Time slewing of coincidence circuit, 1 nano second,  
for NIM inputs between -12 and -36 Usec.  
Relative simultaneity of Data inputs: 200 ps.  
Simultaneity of Data and Strobe inputs: 1 usec.

### FRONT PANEL

16 data inputs,  
1 gate input,  
1 clear input,  
All inputs via LEMO Connectors,  
LED displays for N, L and L Enable.

### CAMAC

#### COMMANDS

NA(0)F(0)	Read Data Registers,	Q=1,
NA(0)F(2)	Read Data Registers; Reset the Data, and LAM registers on S2,	Q=1
NA(0)F(8)	Test LAM	Q=1 if set
NA(15)F(8)	Test LAM	Q=1 if set
NA(0)F(9)	S2 Clear Data and LAM registers	Q=1,
NA(0)F(10)	Clear LAM	Q=1
NA(0)F(24)	Disable LAM,	Q=1,
NA(0)F(25)	S1 Set all data registers & the LAM register to 1,	Q=1,
NA(0)F(26)	Enable LAM,	Q=1,
NA(0)F(27)	Test LAM status,	Q=1, if se
NA(13)F(27)	Test LAM Enable status,	Q=1 if set