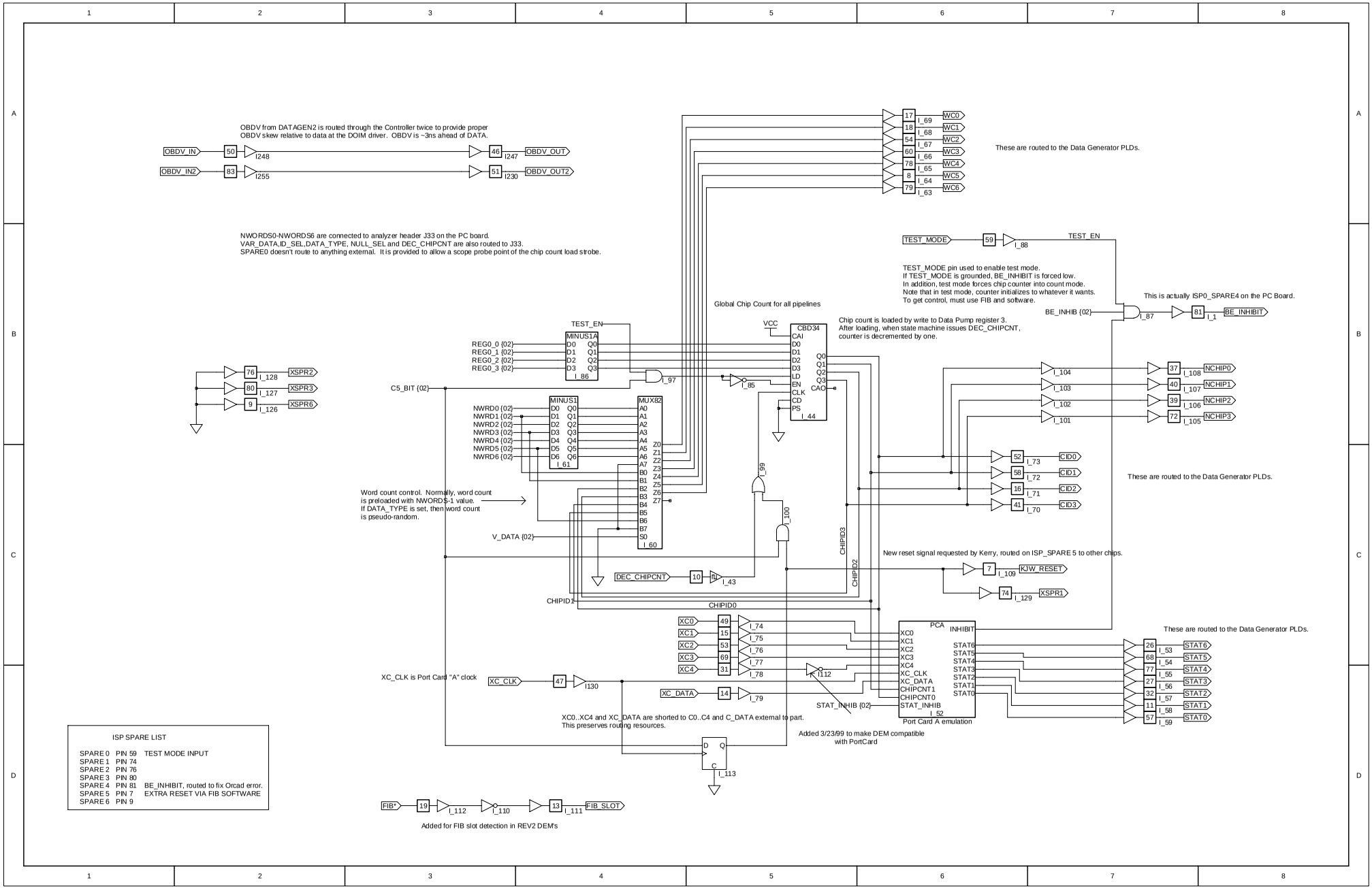
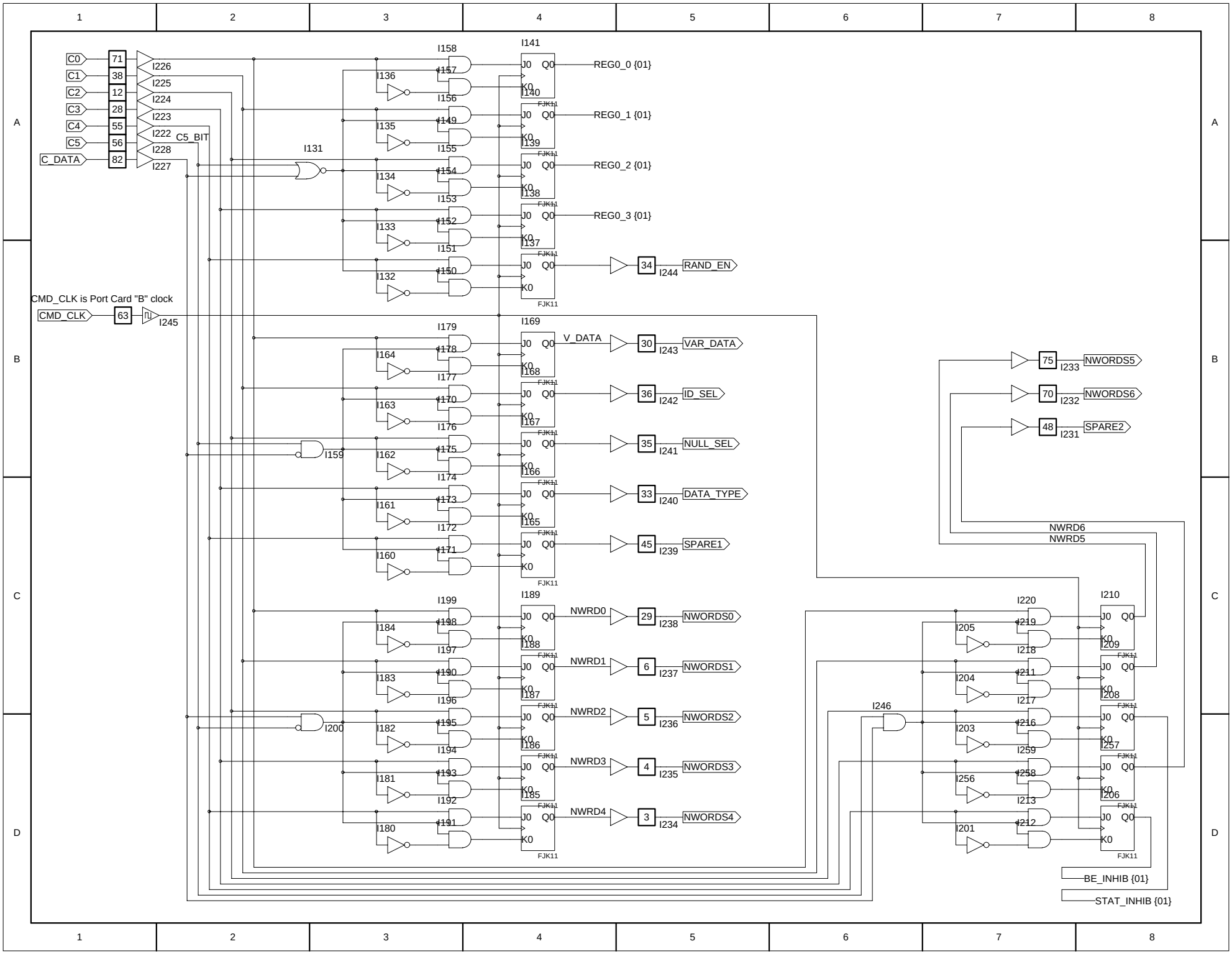

OBDV from DATAGEN2 is routed through the Controller twice to provide proper OBDV skew relative to data at the DOIM driver. OBDV is ~3ns ahead of DATA.
OBDV_IN
OBDV_IN2
OBDV_OUT
OBDV_OUT2
These are routed to the Data Generator PLDs.
NWORDS0-NWORDS6 are connected to analyzer header J33 on the PC board.
VAR_DATA,ID_SEL,DATA_TYPE, NULL_SEL and DEC_CHIPCNT are also routed to J33.
SPARE0 doesn't route to anything external. It is provided to allow a scope probe point of the chip count load strobe.
TEST_MODE
TEST_EN
TEST_MODE pin used to enable test mode.
If TEST_MODE is grounded, BE_INHIBIT is forced low.
In addition, test mode forces chip counter into count mode.
Note that in test mode, counter initializes to whatever it wants.
To get control, must use FIB and software.
This is actually ISP0_SPARE4 on the PC Board.
BE_INHIB {02}
BE_INHIBIT
Global Chip Count for all pipelines
Chip count is loaded by write to Data Pump register 3.
After loading, when state machine issues DEC_CHIPCNT, counter is decremented by one.
VCC
CBD34
MINUS1A
MINUS1
MUX82
REG0_0 {02}
REG0_1 {02}
REG0_2 {02}
REG0_3 {02}
C5_BIT {02}
NWRD0 {02}
NWRD1 {02}
NWRD2 {02}
NWRD3 {02}
NWRD4 {02}
NWRD5 {02}
NWRD6 {02}
V_DATA {02}
Word count control. Normally, word count is preloaded with NWORDS-1 value.
If DATA_TYPE is set, then word count is pseudo-random.
DEC_CHIPCNT
CHIPID0
CHIPID1
CHIPID2
CHIPID3
NCHIP0
NCHIP1
NCHIP2
NCHIP3
CID0
CID1
CID2
CID3
These are routed to the Data Generator PLDs.
New reset signal requested by Kerry, routed on ISP_SPARE 5 to other chips.
KJW_RESET
XSPR1
XSPR2
XSPR3
XSPR6
XC0
XC1
XC2
XC3
XC4
XC_CLK is Port Card "A" clock
XC_CLK
XC_DATA
XC0..XC4 and XC_DATA are shorted to C0..C4 and C_DATA external to part.
This preserves routing resources.
PCA
INHIBIT
STAT6
STAT5
STAT4
STAT3
STAT2
STAT1
STAT0
CHIPCNT1
CHIPCNT0
STAT_INHIB
STAT_INHIB {02}
Port Card A emulation
Added 3/23/99 to make DEM compatible with PortCard
These are routed to the Data Generator PLDs.
FIB*
FIB_SLOT
Added for FIB slot detection in REV2 DEM's
ISP SPARE LIST
SPARE 0 PIN 59 TEST MODE INPUT
SPARE 1 PIN 74
SPARE 2 PIN 76
SPARE 3 PIN 80
SPARE 4 PIN 81 BE_INHIBIT, routed to fix Orcad error.
SPARE 5 PIN 7 EXTRA RESET VIA FIB SOFTWARE
SPARE 6 PIN 9


C0
C1
C2
C3
C4
C5
C_DATA
71
38
12
28
55
56
82
I226
I225
I224
I223
I222
I228
I227
C5_BIT
I131
I158
I157
I156
I149
I155
I154
I153
I152
I151
I150
I136
I135
I134
I133
I132
I141
I140
I139
I138
I137
REG0_0 {01}
REG0_1 {01}
REG0_2 {01}
REG0_3 {01}
FJK11
J0
Q0
K0
34
I244
RAND_EN
CMD_CLK is Port Card "B" clock
CMD_CLK
63
I245
I179
I178
I177
I170
I176
I175
I174
I173
I172
I171
I164
I163
I162
I161
I160
I159
I169
I168
I167
I166
I165
V_DATA
30
I243
VAR_DATA
36
I242
ID_SEL
35
I241
NULL_SEL
33
I240
DATA_TYPE
45
I239
SPARE1
75
I233
NWORDS5
70
I232
NWORDS6
48
I231
SPARE2
NWRD6
NWRD5
I199
I198
I197
I190
I196
I195
I194
I193
I192
I191
I184
I183
I182
I181
I180
I200
I189
I188
I187
I186
I185
NWRD0
NWRD1
NWRD2
NWRD3
NWRD4
29
I238
NWORDS0
6
I237
NWORDS1
5
I236
NWORDS2
4
I235
NWORDS3
3
I234
NWORDS4
I220
I219
I218
I211
I217
I216
I259
I258
I213
I212
I205
I204
I203
I256
I201
I246
I210
I209
I208
I257
I206
BE_INHIB {01}
STAT_INHIB {01}