1. DESCRIPTION

1.1. FUNCTIONAL DESCRIPTION

The Model C117B HIGH SPEED (H.S.) CAENET CAMAC CONTROLLER has been designed to control an H.S. CAENET network through the CAMAC bus. It houses an H.S. CAENET Node and a Control Logic (microprocessor based) which integrates the functions of Node controller and Network error handler.

Standard CAMAC functions allow the User to easily control the serial communication on the H. S. CAENET network according to the typical MASTER/SLAVE communication protocol, where the CAMAC Crate Controller assumes the MASTER function.

It is composed of a collection of registers for the operation control, and two memory buffers for the transmitted and received data packets, arranged in a 16 bit FIFO 256 words deep.

When the H.S. CAENET operation fails, the on-board Control logic generates error messages that are stored in the memory buffer for the received data.

As soon as the data packet (or the error message) is available in the receive buffer, a LAM signal is generated (if enabled).

The communication line uses a simple 50 Ω coaxial cable as a physical medium.

The data transfer rate is 1 MBaud.

(A functional Block Diagram is shown in Fig. 1.1.

2. SPECIFICATIONS

2.1. PACKAGING

Single width CAMAC module.

2.2. EXTERNAL COMPONENTS

(Refer to Fig. 2.1).

CONNECTORS

- No. 1 "SERIAL LINE" LEMO 00 type, 50 Ω connector;
connector for the H.S. CAENET communication line.
The "DATA" LED is On when the H.S. CAENET Node is active.

DISPLAYS

- No.1 "DATA" red LED;
is On when the H.S. CAENET Node is active.

SWITCHES

- No.1 "RESET" push button; by pushing this button
the C117B enters in restart mode; this causes the following operations:

  - the buffers are cleared;
  - the LAM is cleared;
  - the LAM is disabled;
  - every data transfer is aborted;
  - the C117B does not accept any commands.

It remains in this status for about 3 msec.

2.3. POWER REQUIREMENTS

+ 6V	1.2 A

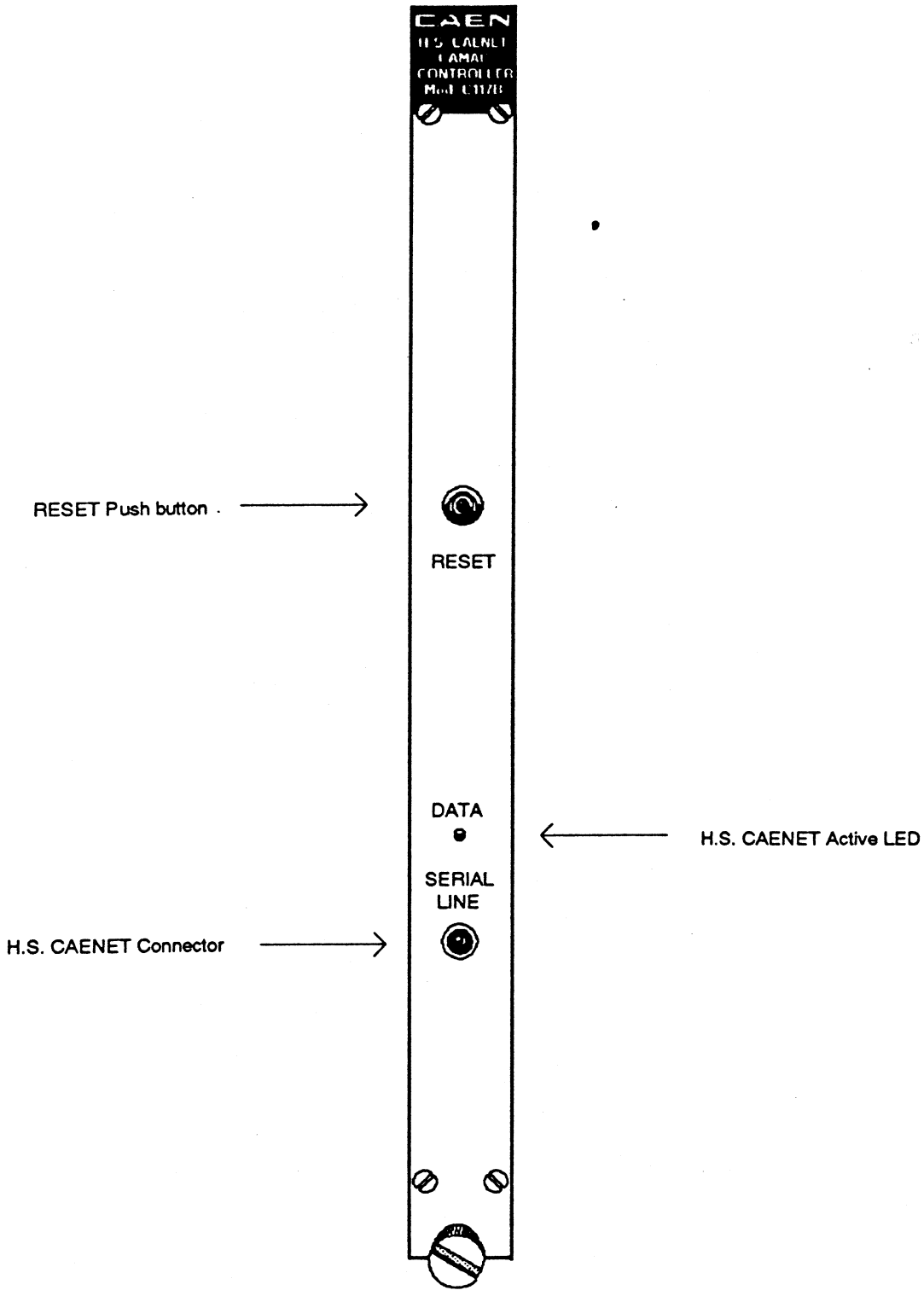

Fig. 2.1: Mod. C117B Front Panel