

**JOERGER ENTERPRISES, INC.****INPUT/OUTPUT REGISTER, MODEL IR**

The Model IR is a Camac compatible module that will perform as a dual 24 bit input register and in addition, contains an optional 24 bit output register in three ways; continuous, strobed, and single event. This last method is internally enabled and will lock the data in after update until the data has been read out. A LAM is generated when the registers are clocked to indicate data update. An output signal, Acknowledge, is generated whose leading edge indicates that the registers have been clocked. The trailing edge indicates that the data has been read. This is useful in interlocking data transfer.

Visual display of all 48 bits is available as an option.

**SPECIFICATION:**

**INPUTS** (all inputs biased to Logic "0" with 10K ohm pullup)

Data, 48 bits  
 Input Impedance 1 TTL load  
 Logic "1" +.8v max.  
 Logic "0" +2v min.

Strobe In (Channel 0, Channel 1)  
 Same as data, trailing edge triggers LAM.

Note: To insure error free readout of data, the input register clocks are inhibited whenever the module is addressed on its "N" line.

**OUTPUTS**

Acknowledge, (Channel 0, Channel 1)  
 This signal is equivalent of LAM, TTL levels, 16ma current sink.

Output Data (Optional)  
 24 Data Bits  
 Logic "0" +2.4v min.  
 Logic "1" +.5v max., sinking 16ma

Update Output (Optional)  
 A pulse equal to F16(S1) is generated for Channel 0 and Channel 1 to indicate output register update. Same levels as Data.

**INDICATORS**

"N" Light Indicates module is addressed.  
 Data Lights 48 LED's to visually indicate contents of input registers, (optional).