



MODEL 40 DUAL 24-BIT OUTPUT REGISTER

The Jorway Model 40 Output Register provides for up to 48 bits of data to be extracted from the dataway 'write' lines for external use. The data is stored in two 24-bit registers. The registers for each channel can be overwritten with command F16•S1 and the appropriate subaddress. This will provide D.C. Level data outputs. Pulsed outputs can be generated by the use of command F17. The data registers will again be overwritten at S1 but will be reset at S2.

Each time a channel is overwritten a "Data Update" pulse is generated. In response to F16 it is approximately 3 μ sec. long. For command F17 the pulse width is the time from S1 to S2.

The data outputs are open collector and capable of sinking 50ma. An inhibit command is provided that can inhibit these data outputs to the front panel connectors. An "N" light is provided to visually indicate when the module has been addressed.



MODEL 40 SPECIFICATIONS

Number of Channels	2
Data Outputs	Each output is from a TTL, open collector driver capable of sinking 50ma at 0.5v (Pull ups can be to a max. of 5.5v.) Optional Totem Pole TTL outputs are available.
Data Update	A logic "1" pulse is generated for the appropriate channel each time its register is updated. Pulse width in response to F16 is approximately 3 μ sec. For F17 it is the time from S1 to S2.
Inhibit Input	A data inhibit signal input is provided for each channel. A logic "1" signal will inhibit the 24 bits for data in that channel. This input is internally biased to logic "0", so with no signal on this line, data will be available at the connector.

MODEL 40 SPECIFICATIONS – Continued

DATAWAY COMMANDS (all fully decoded)

N•F16•A0•S1 and
N•F17•A0•S1

Overwrite channel "0's" 24 Bit data register with information from Write lines, W1 – W24. Triggers a Data Update 0 pulse.

N•F17•A0•S2

Resets the channel 0 data register and returns the data update signal to zero.

Note: The above commands are identical for Channel 1, substituting A1 for A0.

DATAWAY CONTROLS

Z•S2

Resets both channel 0 and channel 1 data registers, and returns both data update signals to zero.

DATAWAY INPUTS

Q

A Q response is generated in response to N•F16•(A0 + A1) and N•F17•(A0 + A1).

INDICATORS

An "N" light is provided to visually indicate when the module is addressed. This signal is integrated so as to respond to narrow pulses.

OPTION 1. Data Outputs can be supplied with TTL Totem Pole outputs capable of sinking 50ma.

POWER REQUIREMENTS

+6v, 710ma, nominal

TEMPERATURE RANGE

0° to 60° C

SIZE

Single width CAMAC module with protective side shields.

PIN IDENTITY

A multipin connector, Cannon Type 20A31P, is used for each of the two channels with the following pin identity:

Pins 1 – 24

Data Outputs corresponding to W1 – W24

Pin 26

Inhibit Input

Pin 27

Data Update Out

Pin 31

Ground

0971