



MODEL 61, 61-1 DUAL PARALLEL INPUT GATES

The Jorway Model 61, Dual Parallel Input Gate is a single width CAMAC compatible module which meets the requirements of EUR 4100e. The module consists of two, independent, 24-bit channels which provide the capability of reading 48 bits of data onto the CAMAC Dataway. External data inputs to each channel are separately integrated to suppress noise.

An external data strobe, applied to each channel, will set the channel's Data Received and LAM flip flops. The strobe input is also integrated to eliminate noise. A Data Received flag is sent back to the data source to indicate that data has been received. Since the data is not placed into storage, for correct operation the input data must remain stable until a Read Command is generated.

Function and subaddress codes are fully decoded and commands are generated for each channel for reading the 24 data bits of each channel onto the Dataway, resetting LAM and Data Received flags of each channel and enabling or disabling L and Q outputs.

Read commands, generated for each channel, will read input data onto the read lines of the Dataway. Such a command, for either channel, will always generate a Q response and will also signal the data source that the data has been read by returning that channel's Data Received flag to zero at time S2. At the same time, the channel's LAM flip flop is also reset.

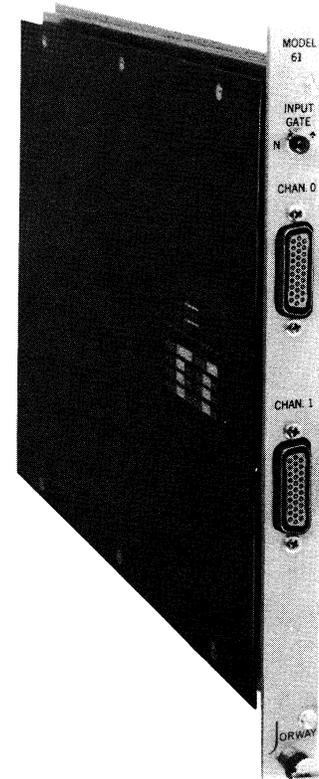
In response to commands F8 and F10, a Q response will be generated if the LAM flip flop has been set and the channel is enabled. An L response will be generated whenever the LAM flip flop is set and the channel is enabled. Busy (B) and P1 can suppress the L output.

Two identical front panel input connectors, one for each channel, are provided. An internally fused +6V output is available at each connector for operation of external equipment.

The Model 61-1 Parallel Input Gate is also a single width CAMAC compatible module which meets the requirements of EUR 4100e. The module is similar to the Model 61 and consists of two, independent 24-bit channels which provide the capability of reading 48 bits of data onto the CAMAC Dataway. External data inputs to each channel are separately integrated to suppress noise.

Read commands, for each channel, will read input data onto the read lines of the Dataway and will generate a Q response.

No interlock between the module and data source is provided. Therefore, the Model 61-1 does not have strobe, Data Received, LAM, Enable/Disable or logic circuitry (other than Read) described for the Model 61.



MODEL 61 SPECIFICATIONS

NUMBER OF CHANNELS

2

SIGNAL INPUTS (each Channel) Inputs internally biased to logic '0'.

Front Panel Data (Note 1)

'0' State +2.0 to +5.5V

'1' State 0 to +0.8V

Strobe, External (Model 61 only) (Note 2)

'0' State +2.0 to +5.5V

'1' State 0 to +0.8V

NOTES

1. Each data bit integrated for ~ 500 nanoseconds to suppress noise.
2. Each strobe signal integrated for ~ 500 nanoseconds; links are provided to increase integration time to approximately 1 millisecond, if required.

DATAWAY CONTROLS (Model 61 only)

Z-S2

Resets both LAM flip flops, both Enable/Disable flip flops and returns both "Data Received" signals to zero.

B

Suppresses L output.

P1

Suppresses L output.

DATAWAY OUTPUTS

Data (R1 through R24)

24-bits of data for each channel.

Status

Q

Q response always generated when Channel 0 to 1 is read. For F8 and F10, a Q response is generated if a channel's LAM flip flop is set and that channel enabled.

L (Model 61 only)

An L signal is generated when either LAM flip flop is set and its channel enabled.

OUTPUT, EXTERNAL

Data Received (Model 61 only)

'0' State: +3.0V to +5.5V

'1' State: 0 to +0.5V

Power Out (fused)

+6V, 300 ma.

Front Panel N Lamp

Indicates Module is addressed.

DATAWAY COMMANDS (All Fully Decoded)*

N·F0·A0

The following commands are used on Model 61

N·F0·A0·S2

N·F8·A0

Read Channel 0 data onto Dataway (24 bits), generates a Q response.

only

Reset Channel 0 LAM flip flop, and return Data Received flag to '0'.

Test Channel 0 LAM flip flop; generates Q response if channel enabled, and LAM flip flop set.

N·F10·A0

Same as F8 except at S2 resets Channel 0 LAM flip flop.

N·F24·A0·S2

Resets Channel 0 Enable/Disable flip flop; disables L and Q signals channel.

N·F26·A0·S2

Sets Channel 0 Enable/Disable flip flop; enables L and Q signals channel; resets Data Received Channel 0 flip flop.

*Note: performs same function on Channel 1 using decoded subaddress A1 in place of A0

POWER REQUIREMENTS

+6V, 300ma nominal Model 6.1-1

+6V, 420ma nominal Model 61

TEMPERATURE RANGE

0° to 60°C

SIZE

Single CAMAC width; protective side sheilds.

PIN IDENTITY (Same For Each Channel) Connector Cannon Type 2DA31P (Mating half is Cannon Type 2DA31S)

Pins 1-24

Data Input (lines are biased to "0" state).

Pin 26

Data Strobe Input (Model 61 only)

Pin 27

Data Received Output (Model 61 only)

Pin 29

+6V out (via 300ma fuse, internal)

Pin 31

Ground