

Technical Information

GENERAL DESCRIPTION

LRS Model 2226A Quad Time-to-Digital Converter provides four identical channels for measuring nanosecond time intervals.

The Model 2226A has one common start input and four stop inputs. Each channel measures the time interval from the leading edge of the common start pulse to the leading edge of its stop signal. The measurement is then converted into a 9-bit binary number which is held in a register for data readout.

A fast start inhibit is provided to control acceptance of start pulses and permit rejection of start pulses which, on the basis of external criteria, do not correspond to desired events. All inputs are operated by standard NIM fast logic levels. The stop inputs are internally gated by the start circuitry in such a way that stop pulses not preceded by start pulses are completely rejected, unless the stop pulse happens to overlap the leading edge of the start pulse. Start pulses not followed by stop pulses will result in an overflow flag on the 10th binary bit.

Each channel of the 2226A uses a stable constant current source to charge a storage capacitor for the time interval between the start and stop signals. This capacitor is discharged at a linear rate by another current source. The time interval is digitally measured by scaling a 40 MHz crystal clock in a 9-bit binary scaler. Clock pulses are accumulated from the time of the start pulse to until the time the storage capacitor has been completely discharged. The binary number is directly calibrated in nanoseconds.

Full scale of the Model 2226A is switch-selectable on the front panel between 102 ns (200 ps/bit) and 510 ns (1 ns/bit). A front-panel switch provides a manual clear and allows the CAMAC Inhibit to be disabled.

A built-in test circuit generates internal Start-Stop commands to all channels to simulate front-panel input pulses with approximately 80 ns spacing. This circuit is triggered by the Increment command independent of the condition of Inhibit.

The Model 2226A TDC is a member of LRS's CAMAC Series, a growing line of instruments which combine high performance with the flexibility and computer compatibility of the CAMAC standard.

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SPECIFICATIONS

Stop Inputs:	4, one per channel; 50 Ω impedance; LEMO (or BNC) connector; direct-coupled; protected to ± 50 volts; input amplitude required > -600 mV; reflections typically $<10\%$; minimum pulse width acceptable at threshold, 6 ns (measured at nominal threshold of 400 mV).
Start Input:	One per module, common to all channels; 50 Ω impedance; protected to ± 50 volts; input amplitude required, > -600 mV. Enables "Busy" latch, which inhibits subsequent "Start" input pulses; minimum pulse width acceptable at threshold, 6 ns (measured at nominal threshold of 400 mV).
Start Inhibit Input:	One, common to all channels; 50 Ω impedance; negative fast logic level (> -600 mV) inhibits "Start" input for duration of inhibit signal. High impedance option available.
Full Scale Time Range:	9-bit binary output corresponds to 102 ns or 510 ns depending upon state of front panel range switch.
Linearity:	Within ± 2 counts from best straightline, 10% of 90% of full scale (± 3 counts, 6% to 100%). (See curve below).
Time Resolution:	One part in 510 of full scale (one bit); on 102 ns range, 200 ps resolution; on 510 ns range, 1 ns resolution.
Conversion Time:	12 us; conversion is initiated by receipt of start input.
Temperature Coefficient:	+ 0.1 to - 0.3 counts per degree C (from 30°C to 70°C).
Manual Clear:	Front panel switch clears all channels and "Busy" latch.
Digital Characteristics:	10-bit TTL incrementing storage registers.
Output:	9 bits plus overflow bit for a single channel presented in parallel to the first 10 "Read" data lines. Logical "1", 0 V; Logical "0", + 5 V.
CAMAC Commands:	Z or C: All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S ₂ ". I: "Start" input is inhibited during CAMAC "Inhibit" command. "Inhibit" can be manually disabled by front-panel switch. Q: A Q=1 response is generated in recognition of an F0, F2, F9, or F25 function for a valid "N" and "A", but there will be no response (Q=0) under any other condition. X: Any =1 (Command Accepted) response is generated when a valid F, N, and A command is generated.