

# Technical Information

## GENERAL DESCRIPTION

The LRS Model 2243 Multi-Mode Linear Analog-To-Digital Converter is optimized to digitize either the amplitude or area of nanosecond analog signals occurring within an externally determined gate interval.

The input signals used with the Model 2243 are typically generated by fast photomultiplier tubes. The instrument analyzes such pulses directly, without preprocessing or preshaping of any kind. Because it accepts positive inputs as well as negative, the Model 2243 allows the superior linearity frequently available in the positive pulse from the last dynode of the photomultiplier tube to be used, leaving the negative anode pulse free for timing and logic purposes. The Model 2243 can also measure nanosecond time intervals by digitizing the pulse overlap of discriminator timing signals presented to the gate and analog signal input.

The input gate of the ADC is normally closed and signal pulses are completely rejected with no resulting deadtime. When the input is enabled by a gate signal of  $-750$  mV, the waveform is accepted and digitization begins. The resolution of the 2243 is 8 binary bits or 0.4% of full scale.

In the area mode, the full scale is  $\pm 150$  picocoulombs, or  $\pm 7.50$  volt-nanoseconds. The width of the analog signal may be either the width of the pulse itself or the effective width generated by opening and closing the linear gate during a signal of longer duration.

The peak mode is intended for use where the signal remains at the peak value for at least 100 nanoseconds. In this mode, the Model 2243 will not begin to digitize the analog input until the time derivative of the charging current equals zero, indicating the peak amplitude of the pulse. Full scale in this mode is  $\pm 1.0$  volts.

A built-in test circuit injects approximately 120 picocoulombs (80% of full scale) into the input circuits to simulate an actual front panel gate and input

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condition. This circuit is triggered by the Increment command independent of the condition of the Inhibit.

The Model 2243 is a member of LRS's CAMAC Series, a growing line of instruments which combine high performance with the flexibility and computer compatibility of the CAMAC standard.

## THEORY OF OPERATION

The Model 2243 digitizes the analog signal by the Wilkinson rundown method. An integrating input capacitor generates a ramp which is used to gate a 40 MHz clock into an 8-bit binary register. The clock pulse train is generated in phase with the control signal; therefore, no  $\pm 1$  count uncertainty is introduced into the conversion. Total conversion time is determined by both speed of the clock and magnitude of the signal to be digitized. Conversion time of the Model 2243 is 25 ns per channel, or 6.4 microseconds for a full scale input.

The accumulated count proportional to the analog input is stored in the instrument's built-in 8-bit binary register until the CAMAC command F(0) causes the digital number to be presented on the parallel data lines. Control and data lines enter the CAMAC Dataway, permitting the use of the 2243 with other CAMAC scalars, input registers, latches, time to digital converters, etc., for readout into a common data recorder. The Model 2243 is completely compatible with the LRS Model 2152 Readout Controller, as well as Type A Interfaces and controllers of other manufacturers.

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## SPECIFICATIONS

Full Scale Input:	Area Mode: 150 pc ( $\pm 1$ volt for 7.5 ns or equivalent). Peak Mode: $\pm 1$ volt ( <u>minimum pulse duration approx. 100 ns</u> ).
Input Impedance:	50 $\Omega$ .
Linear Gate Characteristics:	Normally off; - 750 mV or greater enables; 50 $\Omega$ impedance; 3 ns opening and closing time; direct-coupled; no rate limitations; feedthrough threshold greater than 25 volts.
Linearity:	Better than 1% integral.
Stability:	Better than one channel long-term.
Resolution:	8 binary bits (one part in 256).
Conversion Time:	25 ns x channel number (1 through 256).
Clock Type:	40 MHz cable-controlled oscillator.
Data Readout:	The proper CAMAC function and address command gate the 8 binary data bits and the 1 overflow bit onto the $2^0$ to $2^8$ CAMAC dataway bus lines. Logical 1, < 0.5 volts (0 to 16 mA); Logical 0, open circuit (<100 $\mu$ A at 5.5 volts).
Overflow Output:	Available both as 9th data bit (See "Data Readout") and as an ungated open collector output available for connection to patch pins. Logic levels same as Data Levels above.
Busy Output:	Present from the time of arrival of an accepted analog input pulse until unit is cleared after readout. Buffered open collector output available for connection to patch pins. Logic levels same as Data Levels above.

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Data Ready Output:	Present as soon as conversion is complete; removed when unit is cleared. Buffered open collector output available for connection to patch pins. Logic levels same as Data Levels above.
CAMAC Commands:	Z or C: ADC is cleared by the CAMAC "Clear" or "Initialize" command; requires $S_2$ . I: "Gate" input is inhibited during CAMAC "Inhibit" command. "Inhibit" can be manually disabled by front-panel switch. Q: A $Q=1$ response is generated in recognition of a "read" (F(0)) function for a valid "N" and "A(0)", but there will be no response ( $Q=0$ ) under any other condition.
CAMAC Function Codes:	F(0): Read Group 1 register; requires "N" and "A(0)"; gates 9-bit data to Read Dataway. F(9): Clear Group 1 register "N", "A(0)", and "S <sub>2</sub> "; clears 9-bit data register and Busy Latch. F(25): Increment; requires "N" and "S <sub>2</sub> "; triggers internal test circuit to simulate 6.0 volt-nanosecond input.
Manual Clear:	Front-panel switch allows clearing of ADC.
Packaging:	Single-width CAMAC module.
Power Requirements:	+6V    320 mA                    +24V    150 mA -6V    75 mA                        -24V    45 mA