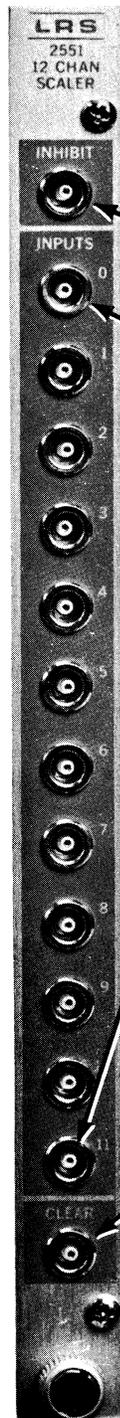


3.240

CAMAC Model 2551 / 2552 12-Channel 100 MHz Scaler



Inhibit inputs 50 Ω , NIM levels, 5 nsec minimum width, must precede inputs by 10 nsec, inhibit interval equals inhibit signal plus 5 nsec.

Channel Inputs: NIM level, 50 Ω , 5 nsec minimum width, DC coupled, 10 nsec double pulse resolution, disabled by Inhibit (front panel or CAMAC)

Any odd numbered channel can be cascaded with any even numbered channel to increase counting capacity.

Clear Input: 50 Ω , NIM levels, 50 nsec minimum width, requires 1 μ sec settling time (during which inputs are inhibited).

Power consumption: +6 V @ 1.2 A
-6 V @ 100 mA

1.75 A
200 mA

7.8 W

9.9

FUNCTIONAL DESCRIPTION

The Model 2551 [2552] consists of twelve 24-bit [16-bit] scaler channels and associated control circuitry. Referring to the block diagram, the Model 2551 circuitry is seen to be divided into four basic parts:

The twelve Scaler channels.

The Inhibit circuit.

The Clear, Increment and LAM Logic.

A CAMAC Control and Address section.

Each of the above parts will be discussed briefly.

The 12 Scaler channels: Each scaler channel is made up of an input translator stage, two high speed flip-flops and two halves of two dual scaler hybrids. The input translator is a common base stage used to convert the NIM pulses to TTL level. This is followed by two J-K flip-flops which divide the input rate by 4 to a maximum of 25 MHz acceptable by the SC100 or SC103 hybrid scalers. Each hybrid scaler contains two parallel scalers and a common tri-state multiplexer. Each scaler channel uses half each of two hybrids connected in series. The first scaler hybrid is a SC-100 dual 11 bit scaler whose 11th bit supplies output pulse via an emitter follower to a second SC-100 [SC-103] this second hybrid provides the remaining 11 [3] bits of the 24 [16] bit channel. The 11th [3rd] bit of this hybrid drives the overflow OR gate consisting of twelve emitter followers, one for each channel, with their emitters tied common.

As a user option, the output of the last bit of any even-numbered channel can be tied back to the next (odd-numbered) channel's first J-K flip-flop inputs. This connection provides for a single 48-bit [32-bit] scaler channel.

In the 2551 module only one channel can be strobed at a time. The first two J-K flip-flops each require separate open collector gates with the outputs tied common and inverted to become the two least significant bits of the output gates.